REMARKS

Reconsideration of this application as amended is respectfully requested.

In the Office Action, claims 1-14 and 17-24 were pending. Claims 1-14 and 17-24 were rejected. In this response, claims 3-4 and 21 have been canceled without prejudice. Claims 1-2, 5-6, 8, 13-14, and 17-20 have been amended. Replacement sheets of Figures 2, 4-7, and 9 have been submitted. No new matter has been added.

Claims 13-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In view of the foregoing amendments, it is respectfully submitted that the rejections have been overcome.

Claims 1-24 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-25 of copending Application No. 09/748,825 (042390.P8645). Claims 1-24 are also provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of copending Application No. 09/749,133 (042390.P10825). Terminal disclaimers have been submitted herein.

Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Intel Corporation Application Note AP-629 or AP-678, each taken separately, in view of Olivo et al. In view of the foregoing amendments, it is respectfully submitted that claims 1-2, 5-14, and 17-24 include limitations that are not disclosed or suggested by the cited references.

Specifically, independent claim 1 recites as follows:

> 1. A method comprising:
>
> enabling a special programming mode of a memory by entering a special programming access code in a state controller, wherein the memory includes automation circuitry for internal program verification and

wherein enabling special programming mode disables the internal program verification by the automation circuitry of the memory;

programming a plurality of words into the memory during the special programming mode without having the automation circuitry of the memory to perform the internal program verification;

exiting the special programming mode of the memory after the plurality of words have been programmed into the memory; and

enabling the internal program verification of the memory after exiting the special programming mode, wherein one or more words subsequently programmed into the memory are verified by the internal program verification performed by the memory.

(Emphasis added)

Independent claim 1 includes limitations that when a memory enters a special programming mode, an internal verification performed by the memory is disabled. Rather, an external verification processor (e.g., a host or ATE) is used to verify the words being programmed into the memory during the special programming mode. Thereafter, when the memory exits the special programming mode (e.g., going back to a normal mode), the internal verification is enabled and any subsequent words programmed into the memory are verified by the internal verification performed by the memory (rather than the external ATE). It is respectfully submitted that the above limitations are absent from the cited references, individually or in combination.

Rather, both AP-629 and AP-678 disclose or suggest eliminating the external verification operations. That disclosure teaches away from the amended claim 1. Specifically, the AP-629 discloses the following:

"The flash memory internal Write State Machine (WSM) automatically verifies data written to the memory. Program verify operations initiated by the ATE are redundant with flash memory internal program verify operations. You can save time by not performing program verify operations with the ATE."

(AP-629 page 9, col. 2, emphasis added).

An ATE (automatic test equipment) is an external testing system outside of the memory itself as disclosed by AP-629 (see, pages 5-6, Fig. 1 of AP-629). That is, the AP-629 clearly discloses or suggests eliminating the external verification operations, rather than the internal verification operations, which clearly teaches away from the present invention as claimed.

Although the Examiner acknowledges that none of the Intel references teaches disabling internal program verification operations during "special" programming mode so that a plurality of words is programmed in the "special" or test mode without the memory performing internal program verification (7/16/2004 Office Action, page 9), the Examiner maintains that Olivo discloses such limitations. Specifically, the Examiner stated:

> "Olivo similarly discloses a method of programming a memory such as a flash nonvolatile memory during a "special" or test programming mode of the memory, and teaches disabling program verification operations by an internal state machine during the "special" programming mode so that a plurality of words may be programmed or tested without the memory performing internal program verification (see column 1, lines 26-62; column 2, lines 9-31; and column 4, lines 7-12 and 32-36, e.g.)."

(7/16/2004 Office Action, page 10, emphasis added).

Applicant respectfully disagrees. It is respectfully submitted that the test circuitry of Olivo disables the internal state machine, instead of internal program verification of the memory, during the testing (see, col. 2, lines 9-37 of Olivo). It is respectfully submitted that disabling an internal state machine is not the same as disabling internal program verification. There is no mention of disabling internal program verification within the cited section of Olivo as suggested by the Examiner.

In addition, disabling the internal state machine of Olivo is not related to program verification. Rather, by disabling the internal state machine, the addresses occupied by the internal state machine can be used for other purposes, such as testing. Specifically, Olivo stated:

"Consequently, having excluding the internal state machine 11, the addresses can be used freely and, using the above listed control signals with their new meaning, the desired cells can be programmed and their correctness can be verified."

(Olivo col. 4, lines 32-36, emphasis added).

Thus, Olivo fails to disclose or suggest disabling internal program verification. Olivo further states:

"Verification is performed by a comparison of the values present after memory programming with the correct ones supplied through the data bus 3. The signal CEN also returns to a low logic value Vil and the circuit is ready to perform a new test or return to normal operation.

The test method in accordance with the present invention has the following advantages: The memory matrix test can be performed in a manner fully independent of control unit operation. The duration of the programming pulse and that of the verification phase are not bound to the internal time base and can thus be selected at will. The sequence of performance of the actual test is compatible with that used for testing EPROM memories of the known art and thus permits use of the same circuitry equipment for its performance."

(Olivo col. 4, line 63 to col. 5, line 10, emphasis added).

Clearly, these verification operations are performed within the memory (e.g., internal program verification), rather than by an external host processor as claimed in the present invention. Again, there is no mention of disabling internal program verification within the cited section of Olivo as suggested by the Examiner. Such a suggestion can only be found in Applicant's own disclosure. It would be impermissible hindsight to use Applicant's own disclosure to against the Applicant.

Furthermore, there is no suggestion within the cited references to combine with each other. It would be impermissible hindsight, based on Applicant's own disclosure, to combine these references. Even if they were combined, such a combination still lacks the limitations set forth above. Therefore, for the reasons discussed above, it is respectfully submitted that independent claim 1 is patentable over the cited references.

Similarly, independent claim 13 includes limitations similar to those recited in claim 1. Thus, for the reasons similar to those discussed above, independent claim 13 is patentable over the cited references.

Given that the rest of the claims depend from one of the above independent claims, at least for the reasons similar to those discussed above, it is respectfully submitted that the rest of the claims are patentable over the cited references. Withdrawal of the rejections is respectfully requested.

In view of the foregoing, Applicant respectfully submits the present application is now in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned attorney at (408) 720-8300.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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Kevin G. Shao
Attorney for Applicant
Reg. No. 45,095

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025-1026
(408) 720-8300